

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Werner Ertle et al.	Examiner:	Robert T. Huber
Serial No.:	10/522,502	Group Art Unit:	4146
Filed:	November 11, 2005	Docket No.:	1431.124.101/FIN404PCT/US
Title:	SEMICONDUCTOR WAFER WITH ELECTRICALLY CONNECTED CONTACT AND TEST AREAS		

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**RESPONSE TO RESTRICTION REQUIREMENT**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This is responsive to the Office Action mailed March 7, 2008, in which a Restriction Requirement was set forth relative to the Examiner-identified inventions of Group I (claims 18-33 and 38-40, drawn to a semiconductor chip and related devices) and Group II (claims 34-37, drawn to a method of processing a semiconductor wafer). In response, Applicant hereby elects Group I (claims 18-33 and 38-40) without traverse.

Any inquiry regarding this Response should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

Werner Ertle et al.,

By their attorneys,

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